AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Original) A processor comprising:

a branch prediction storage including storage for branch direction indications and associable branch prediction qualifier indications, wherein entries provided for branch direction indications are more numerous than those provided for branch prediction qualifier indications.

2. (***Currently Amended***) The processor of claim 1 wherein, during execution of program code on the processor, at least some of the branch prediction qualifier entries are associated with multiple ones of the branch direction entries.

3. (Original) The processor of claim 1 wherein the branch direction indications and the branch prediction qualifier indications are accessible based at least in part on one or more of instruction instance identifiers and gshare addresses.

4. (Original) The processor of claim 3 wherein the branch prediction qualifier indications are accessible based at least in part on one or more of least significant bits of the instruction instance identifiers and least significant bits of gshare addresses.

5. (***Currently Amended***) The processor of claim 3 wherein the instruction instance identifiers comprise one of ~~include~~ program counters, physical addresses, and virtual addresses.

6. (***Currently Amended***) The processor of claim 1 wherein the branch prediction storage comprises ~~includes~~ storage for one or more of branch history pattern indications and branch target instruction instance identifiers.

7. (***Currently Amended***) The processor of claim 1 wherein the branch direction indications comprise ~~includes~~ one or more bits that indicate one or more of branch history, branch prediction, and branch pattern.

8. (***Currently Amended***) The processor of claim 1 wherein the branch prediction qualifier indications comprise ~~include~~ one or more bits that indicate one or more of confidence, strength, and validity of branch direction indications.

9. (Original) A branch prediction storage that includes entries for branch direction indications and entries for branch prediction qualifier indications, wherein the branch direction indication entries are more numerous than the branch prediction qualifier indications.

10. (Original) The branch prediction storage of claim 9 wherein the branch direction indications and the branch prediction qualifier indications are accessible based at least in part on one or more of instruction instance identifiers and gshare addresses.

11. (Original) The branch prediction storage of claim 10 wherein instruction instance identifiers include physical addresses, virtual addresses, and program counters.

12. (Original) The branch prediction storage of claim 9 wherein the branch prediction storage also includes entries for one or more of branch history patterns and branch target instruction instance identifiers.

13. (Original) The branch prediction storage of claim 9 wherein the branch prediction qualifier indications include one or more bits that indicate one or more of confidence, strength, and validity of branch direction indications.

14. (Original) The branch prediction storage of claim 9 wherein the branch direction indications include one or more bits that indicate whether a branch is taken or not taken.

15. (Original) A method of operating a processor that supports branch prediction, the method comprising:

accessing a branch prediction structure;

determining from the branch prediction structure a branch direction indication that corresponds to an instruction instance identifier; and

determining from the branch prediction structure a branch prediction qualifier indication that corresponds to the instruction instance identifier, wherein the branch prediction structure includes more entries for branch direction indications than entries for branch prediction qualifier indications.

16. (Original) The method of claim 15 wherein determining the branch direction indication and the branch prediction qualifier indication is based at least in part on the instruction instance identifier and at least in part on the least significant bits of the instruction instance identifier, respectively.

17. (Original) The method of claim 16 wherein determining the branch direction indication comprises obtaining one or more values from one or more operations on the instruction instance identifier and selecting the branch direction indication that corresponds to the value.

18. (***Currently Amended***) The method of claim 17 [[16]] wherein determining the branch direction indication comprises selecting the branch prediction qualifier indication with least significant bits of the obtained one or more values.

19. (***Currently Amended***) The method of claim 18 wherein at least some of the least significant bits of the obtained one or more values are unchanged from the instruction instance identifier.

20. (Original) The method of claim 15 further comprising determining one or more of a branch history pattern and a branch target instruction instance identifier that corresponds to the instruction instance identifier.

21. (Original) The method of claim 20 further comprising determining the branch direction indication with the instruction instance identifier and one or more of the branch history pattern and the instruction instance identifier.

22. (Original) The method of claim 15 wherein the instruction instance identifier includes one or more of physical addresses, virtual addresses, and program counters.

23. (Original) The method of claim 15 further comprising performing branch prediction based at least in part on the determined branch direction indication and the determined branch prediction qualifier indication.

24. (Original) The method of claim 15 further comprising updating the branch prediction qualifier indication and the branch direction indication with respect to outcome of the instruction instance that corresponds to the instruction instance identifier.

25. (***Currently Amended***) A method of operating a processor that supports branch prediction, the method comprising:

determining if an instruction instance is a branch instruction and if the instruction instance is represented in a branch prediction structure;

if the instruction instance is a branch instruction and is represented in the branch prediction structure,

selecting in the branch prediction structure a branch direction indication that corresponds to an instruction instance identifier that corresponds with the instruction instance, and

selecting in the branch prediction structure a branch prediction qualifier indication that corresponds to the instruction instance identifier; and

performing branch prediction based at least in part on the branch direction indication and the branch prediction qualifier ~~direction condition~~ indication,

wherein the branch prediction qualifier indication is aliased to multiple branch direction indications.

26. (Original) The method of claim 25 wherein the branch prediction indication is selected based at least in part on one or more of least significant bits of the instruction instance identifier and least significant bits of the gshare address.

27. (Original) The method of claim 25 wherein the instruction instance identifier includes one or more of physical addresses, virtual addresses, and program counters.

28. (Original) The method of claim 25 further comprising updating the branch direction indication and the branch prediction qualifier based at least in part on an outcome of the instruction instance.

29. (Original) The method of claim 25 wherein the branch prediction qualifier indication is one or more bits that indicate one or more of confidence, strength, and validity of branch direction indications.

30. (Original) An apparatus comprising:

a processor; and

means for sharing branch prediction qualifier indications between multiple branch direction indications.

31. (Original) The apparatus of claim 30 further comprising means for updating the branch direction indications and the shared branch prediction qualifier indications.

32. (Original) The apparatus of claim 30 further comprising instruction instance fetching, decoding, and executing means.

33. (Original) A branch predictor comprising:

branch direction entries accessible by first representations that correspond to branch instruction instance identifiers; and

branch prediction qualifier entries accessible by second representations that correspond to the first representations, wherein the branch prediction qualifier entries are fewer than the branch direction entries.

34. (Original) The branch predictor of claim 33 wherein the second representations include least significant bits of the first representations.

35. (Original) The branch predictor of claim 33 wherein the first representations include one or more of physical addresses, virtual addresses, Gshare addresses, program counters, and hashed addresses.

36. (Original) The branch predictor of claim 33 further comprising one or more of branch history pattern entries and branch target instruction instance identifiers.

37. (Original) The branch predictor of claim 36 further comprising a shift register that includes one or more of the branch history pattern entries and the branch target instruction instance identifiers.

38. (Original) The branch predictor of claim 33 wherein the branch prediction qualifier entries host one or more bits that indicate one or more of confidence, strength, and validity of branch direction indications.

39. (Original) An apparatus comprising:

a processor that includes branch prediction storage having entries for branch direction indications and entries for branch prediction qualifier indications, wherein the branch prediction storage has more branch direction entries than branch prediction qualifier entries;

a bus coupled to the processor; and

memory coupled to the bus.

40. (Original) The apparatus of claim 39 wherein the branch direction entries are accessible with values that correspond to instruction instance identifiers and the branch prediction qualifier entries are accessible with least significant bits of those values.

41. (Original) The apparatus of claim 40 wherein the values include physical addresses, virtual addresses, program counters, gshare addresses, and hashed addresses.

42. (Original) The apparatus of claim 40 wherein the values result from one or more operations performed on the instruction instance identifiers.

43. (Original) The apparatus of claim 39 wherein the processor further includes a branch history pattern shift register.

44. (Original) The apparatus of claim 39 further comprising storage devices.